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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/943,078	08/30/2001	Todd R. Abbott	MIO 0083 PA	7688

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EXAMINER	
KIELIN, ERIK J	

ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 05/10/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/943,078	ABBOTT, TODD R.	
	Examiner	Art Unit	
	Erik Kielin	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-7,9,11,14-16,39 and 45-49* is/are pending in the application.

4a) Of the above claim(s) *none* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2-7,9,11,14-16,39 and 45-49* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 17 March 2004 has been entered.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims **7**, 5, 6, 46, 47, 49, and **11** and **14**, 15, and **16** are rejected under 35 U.S.C. 102(b) as being anticipated by US 5,844,274 (**Tsutsumi**).

Regarding claim 7, **Tsutsumi** discloses a method of fabricating a semiconductor device comprising,

forming a first dielectric layer **3**, **33**, **34** over a base substrate **1** (Figs. 1, 56);

forming a damascene trench **4** in said first dielectric layer **3**, **33**, **34**, said damascene trench having a gate area and a local interconnect area wherein said gate area and local interconnect area are formed during a single mask and etch process (Figs. 2, 4, 13);

forming a gate oxide layer **9** on said base substrate **1** within said gate area of said damascene trench **4** (Figs. 7, 68);

depositing a conductive layer **10**, **14** over said base substrate such that said damascene trench is filled with a conductive material (Figs. 8, 11, 13, 68);

planarizing said device to define a damascene structure including a damascene gate structure and a damascene local interconnect structure electrically coupled by said conductive material within said damascene trench wherein said damascene local interconnect structure forms a connection to said base substrate (Figs. 13, 15-17, 19, 20);

removing said first dielectric layer **3**, **33**, **34** (Figs. 45, 48, 50, 51, 54, 55, 60, 65); and

providing at least one implant **5b**, **11**, **13**, **21** within said base substrate through said damascene trench (Figs. 2, 10, 11, 23).

Regarding claim 5, **Tsutsumi** discloses a method of fabricating a semiconductor device according to claim 7, wherein said first dielectric layer **3** formation comprises depositing a conformal interlayer dielectric material over said base substrate (Fig. 1).

Regarding claim 6, **Tsutsumi** discloses a method of fabricating a semiconductor device according to claim 7, wherein said damascene trench is formed by "photolithography and etching" (paragraph bridging cols. 13-14), which inherently comprises,

forming a patterned mask over said first dielectric layer;

etching through said first dielectric layer to said base substrate in areas defined by said patterned mask; and

stripping said patterned mask from said first dielectric layer.

This is inherently "photolithography and etching." (See Van Zant, Microchip Fabrication, 4th ed. McGraw-Hill: New York, 2000, p. 199 for verification.)

Regarding claim 46, **Tsutsumi** discloses a method of fabricating a semiconductor device according to claim 7, further comprising forming a plurality of local interconnect areas in said damascene trench (Figs. 94-99).

Regarding claim 47, **Tsutsumi** discloses a method of fabricating a semiconductor device according to claim 7, further comprising forming a plurality of gate areas in said damascene trench (Figs. 94-99).

Regarding claim 49, **Tsutsumi** discloses a method of fabricating a semiconductor device according to claim 6, wherein said gate area and said local interconnect area of said damascene trench are both formed by said patterned mask and etching (paragraph bridging cols. 3-4).

Regarding claim 11, **Tsutsumi** discloses a method of fabricating a semiconductor device comprising,

forming a first dielectric layer **3, 33, 34** over a base substrate **1** (Figs. 1, 56);

forming a damascene trench **4** in said first dielectric layer **3, 33, 34**, said damascene trench having a gate area and a local interconnect area wherein said gate area and local interconnect area are formed during a single mask and etch process (Figs. 2, 4, 13);

forming a gate oxide layer **9** on said base substrate **1** within said gate area of said damascene trench **4** (Figs. 7, 68);

depositing a conductive layer **10**, **14** over said base substrate such that said damascene trench is filled with a conductive material, wherein said conductive material comprises a polysilicon material (Figs. 8, 11, 13, 50, 68);

planarizing said device to define a damascene structure including a damascene gate structure and a damascene local interconnect structure electrically coupled by said conductive material within said damascene trench wherein said damascene local interconnect structure forms a connection to said base substrate (Figs. 13, 15-17, 19, 20);

removing said first dielectric layer **3**, **33**, **34** (Figs. 45, 48, 50, 51, 54, 55, 60, 65); and

forming a silicide layer over said polysilicon material within said gate area of said damascene trench (col. 17, lines 14-22; col. 23, lines 37-50; Fig. 51).

Regarding claim 14, **Tsutsumi** discloses a method of fabricating a semiconductor device comprising,

forming a first dielectric layer **3**, **33, 34** over a base substrate **1** (Figs. 1, 56);

forming a damascene trench **4** in said first dielectric layer **3**, **33, 34**, said damascene trench having a gate area and a local interconnect area wherein said gate area and local interconnect area are formed during a single mask and etch process (Figs. 2, 4, 13);

forming a gate oxide layer **9** on said base substrate **1** within said gate area of said damascene trench **4** (Figs. 7, 68);

depositing a conductive layer **10**, **14** over said base substrate such that said damascene trench is filled with a conductive material (Figs. 8, 11, 13, 68);

planarizing said device to define a damascene structure including a damascene gate structure and a damascene local interconnect structure electrically coupled by said conductive material within said damascene trench wherein said damascene local interconnect structure forms a connection to said base substrate (Figs. 13, 15-17, 19, 20);

removing said first dielectric layer **3**, **33**, **34** (Figs. 45, 48, 50, 51, 54, 55, 60, 65);; and

forming lightly doped drain regions **11** in said base substrate 1 after removing said first dielectric layer, said lightly doped drain regions formed within said base substrate adjacent to said damascene gate structure **10** and said damascene local interconnect structure **10**, **14** (Figs. 10, 11, paragraph bridging cols. 2-3).

Regarding claim 15, **Tsutsumi** discloses a method of fabricating a semiconductor device according to claim 14, further comprising forming spacers **12** against the vertical walls of said damascene gate structure 10 and said damascene local interconnect structure **10**, **14** (Figs. 10, 11, 13; paragraph bridging cols. 2-3).

Regarding claim 16, **Tsutsumi** discloses a method of fabricating a semiconductor device comprising:

forming a first dielectric layer **3**, **33**, **34** over a base substrate **1** (Figs. 1, 56);

forming a damascene trench **4** in said first dielectric layer **3**, **33**, **34**, said damascene trench having a gate area and a local interconnect area wherein said gate area and local interconnect area are formed during a single mask and etch process (Figs. 2, 4, 13);

forming a gate oxide layer **9** on said base substrate **1** within said gate area of said damascene trench **4** (Figs. 7, 68);

depositing a conductive layer **10**, **14** over said base substrate such that said damascene trench is filled with a conductive material (Figs. 8, 11, 13, 68);

planarizing said device to define a damascene structure including a damascene gate structure and a damascene local interconnect structure electrically coupled by said conductive material within said damascene trench wherein said damascene local interconnect structure forms a connection to said base substrate (Figs. 13, 15-17, 19, 20);

removing said first dielectric layer **3**, **33**, **34** (Figs. 45, 48, 50, 51, 54, 55, 60, 65);; and

forming lightly doped drain regions **11** in said base substrate 1 after removing said first dielectric layer, said lightly doped drain regions formed within said base substrate adjacent to said damascene gate structure **10** and said damascene local interconnect structure **10**, **14** (Figs. 10, 11, paragraph bridging cols. 2-3);

forming spacers **12** against the vertical walls of said damascene gate structure and said damascene local interconnect structure (Figs. 10, 11); and

forming doped source/drain regions **13** in said base substrate **1** after forming said spacers such that said base substrate is doped more deeply into said base substrate adjacent to said spacers than into said base substrate underneath said spacers (Figs. 10, 11).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 2, 3, 45, 48 and **39** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Tsutsumi** in view of the basic text of **Ghandi**, VLSI Fabrication Principles, 2nd ed., John Wiley & Sons: New York, 1994, pp. 452, 456.

Regarding claims 2 and 39, **Tsutsumi** discloses a method of fabricating a semiconductor device comprising:

forming an isolation region **2** in a base substrate **1**;

forming a first dielectric layer **3** over said base substrate **1**;

forming a first patterned mask over said first dielectric layer (Fig. 2);

etching through said first dielectric layer to said base substrate in areas defined by said first patterned mask to define a damascene trench in said first dielectric layer, said damascene trench having a gate area and a local interconnect area, wherein said gate area and local interconnect area are formed during a single mask and etch process, and positioned such that at least a portion of said damascene trench at least partially overlies said isolation trench (Fig. 2; paragraph bridging cols. 13-14; Figs. 45, 48, 50, 51, 54, 55, 60, 65);

stripping said first patterned mask from said first dielectric layer **3** (Fig. 2; the previous 3 steps are inherent in photolithography and etching as explained above with regard to claim 6);

growing an oxide layer **36** on said base substrate, said oxide layer **36** within said gate area of said damascene trench defining a gate oxide layer (Figs. 7, 68);

forming a second patterned mask **33**, **34** over said semiconductor device, said second patterned mask **33**, **34** arranged to expose at least a portion of said oxide layer **36** within said local interconnect area;

etching away the exposed portion of said oxide layer **36** within said damascene trench **4**;

providing at least one contact implant **5b**, **11**, **13**, **21** within said base substrate **1** through said damascene trench (Figs. 2, 10, 11, 23);

stripping said second patterned mask from said semiconductor device (Fig. 68; see also Figs. 58-70 and col. 25, line 1 to col. 26, line 20);

depositing a conductive layer **10**, **14**, **32** comprising a conductive material over said device such that said conductive layer fills said damascene trench 4 (Figs. 13, 68);

planarizing said conductive layer down to the surface of said dielectric layer (Figs. 13, 15-17, 19, 20);

removing said first dielectric layer to define a damascene gate structure and a damascene local interconnect structure **3**, **33**, **34** (Figs. 45, 48, 50, 51, 54, 55, 60, 65);

forming lightly doped drain regions **11** in said base substrate **1** adjacent to said damascene gate structure **10** and said damascene local interconnect structure **10**, **14**, **32**;

depositing a spacer layer **12** over said device;

anisotropically etching said spacer layer such that spacers are formed over the portions of said base substrate where said lightly doped drain regions are formed (Figs. 15-17); and

forming doped source/drain regions **13** in said base substrate **1** after forming said spacers **12** such that said base substrate is doped more deeply into said base substrate adjacent to said spacers than into said base substrate underneath said spacers.

Tsutsumi does not state that the oxide isolation film **2** is a "trench" formed "in" the base substrate **1**.

Ghandi teaches that thermal oxidation of the silicon substrate to form SiO_2 reduces leakage current by reducing surface state density (p. 452, section entitled "7.1 Thermal Oxidation

of Silicon") is better than deposition for forming oxides on a semiconductor substrate to prevent leakage current generated by dangling bonds at the interface. **Ghandi** also teaches that oxidation consumes the silicon substrate in which it is formed, accordingly the isolation trench is formed "in" the substrate by thermal oxidation (p. 456, section entitled "7.1.3 Oxide formation").

It would have been obvious for one of ordinary skill in the art, at the time of the invention to use thermal oxidation of the base substrate **1** of **Tsutsumi** to form the isolation trench **2**, in order to reduce leakage current, as taught by **Ghandi**. Moreover, because **Tsutsumi** is silent to the method by which the isolation trench 2 is formed, one of ordinary skill would be motivated to use the well known method taught in **Ghandi** to reduce time in research developing a new method.

Regarding claims 3 and 45, **Tsutsumi** discloses a method of fabricating a semiconductor device according to claim 2, wherein at least a portion of said damascene trench at least partially overlies said isolation trench **2** (Figs. 45, 48, 50, 51, 54, 55, 60, 65).

Regarding claim 48, **Tsutsumi** in view of **Ghandi** discloses a method of fabricating a semiconductor device according to claim 2, wherein said isolation trench comprises a shallow trench isolation structure. It is seen to be inherent that because the isolation trench is best formed by oxidation according to **Ghandi**, that the trench is shallow because for a 50 nm isolation trench thickness (as disclosed in Tsutsumi at col. 12, lines 53-56), the depth would only be 50 nm/2.27, or about 22 nm deep, as taught by **Ghandi** based upon the amount of silicon substrate consumed during oxidation (Ghandi, p. 456, section entitled "7.1.3 Oxide formation").

5. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over **Tsutsumi** in view of US 6,534,393 B1 (**Zhou** et al.).

The prior art of **Tsutsumi**, as explained above, discloses each of the claimed features except for the formation of the of the trench including the steps of:

etching into said base substrate defining an isolation trench opening in said base substrate; and

filling said isolation trench opening with a dielectric material.

Zhou teaches a method of forming gate electrodes **18A** and interconnect **18** in the same trench (Figs. 7A-7C) and forms a shallow trench isolation **12** by etching into the substrate and filling with dielectric (col. 4, last paragraph).

It would have been obvious for one of ordinary skill in the art, at the time of the invention to form the isolation film 2 of **Tsutsumi** using etching a trench and filling with dielectric because **Zhou** teaches that any filed oxide will work to form an isolation region (col. 4, last paragraph). Moreover, there exists no evidence of record to indicate that the isolation trench formed by etching and filling with dielectric material has any unexpected result over any other art know method of forming an isolation trench.

6. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over **Tsutusmi**.

Tsutsumi discloses a method of fabricating a semiconductor device comprising:

forming a first dielectric layer **3, 33, 34** over a base substrate **1** (Figs. 1, 56);

forming a damascene trench **4** in said first dielectric layer **3**, **33, 34**, said damascene trench having a gate area and a local interconnect area wherein said gate area and local interconnect area are formed during a single mask and etch process (Figs. 2, 4, 13);

forming a gate oxide layer **9** on said base substrate **1** within said gate area of said damascene trench **4** (Figs. 7, 68), wherein said gate oxide-layer formation comprises

growing an oxide layer **36** on said base substrate **1** (Fig. 62);

forming a patterned mask **33**, **34** over said semiconductor device, said pattern arranged to expose at least a portion of said oxide layer **36** within said local interconnect area;

etching away the exposed portion of said oxide layer (Fig. 70), and

stripping said patterned mask from said semiconductor device (Fig. 68; see also Figs. 58-70 and col. 25, line 1 to col. 26, line 20);

depositing a conductive layer **10**, **14**, **32** over said base substrate such that said damascene trench is filled with a conductive material (Figs. 13, 68);

planarizing said device to define a damascene structure including a damascene gate structure and a damascene local interconnect structure electrically coupled by said conductive material within said damascene trench wherein said damascene local interconnect structure forms a connection to said base substrate (Figs. 13, 15-17, 19, 20);

removing said first dielectric layer **3**, **33**, **34** (Figs. 45, 48, 50, 51, 54, 55, 60, 65); and

providing at least one implant **5b**, **11**, **13**, **21** within said base substrate through said damascene trench (Figs. 2, 10, 11, 23).

Tsutsumi does not teach forming the implant **21** (Fig. 23) into the substrate **1** prior to stripping said patterned mask.

However, it would have been obvious for one of ordinary skill in the art, at the time of the invention to leave the patterned mask in place during the implantation to protect the dielectric layer from being implanted with impurities and/or to prevent penetration through the dielectric layer into the substrate yielding undesired implantation regions. Moreover, it has been held that the selection of any order of performing process steps is *prima facie* obvious in the absence of new or unexpected results. See *In re Burhans*, 154 F.2d 690, 69 USPQ 330 (CCPA 1946). No unexpected results are presently of record for this process order.

Response to Arguments

7. Applicant's arguments filed 17 March 2004 have been fully considered but they are not persuasive.

Applicant argues that **Tsutsumi** does not teach the newly added limitation to each of the independent claims recited as, "wherein said gate **area** and local interconnect **area** are formed during a single mask and etch process;" yet this feature is very clearly shown in Fig. 2 of **Tsutsumi**. Simply because additional steps are performed after the formation of the gate **area** and local interconnect **area** to form the gate and interconnect, does not mean that **Tsutsumi** does not anticipate formation of the **areas** in a single mask and etch step.

Applicant also argues **Tsutsumi** does no teach that "the local interconnect area forms a connection to the base substrate." First this is not claimed. Second the instant specification does not teach this either. An "area" cannot make a "connection" because the word "area" merely

defines a region and is an abstract entity incapable of making a connection. Accordingly, this argument is not persuasive.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Erik Kielin whose telephone number is 571-272-1693. The examiner can normally be reached on 9:00 - 19:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr. can be reached on 571-272-1702. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Erik Kielin
Primary Examiner
8 May 2004